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10/604,862	08/22/2003	Ming-Yang Chao	MTKP0032USA	1861

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EXAMINER	
GUPTA, PARUL H	

ART UNIT	PAPER NUMBER
2627	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/604,862	CHAO, MING-YANG	
	Examiner	Art Unit	
	Parul Gupta	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14,18,40 and 43-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,4-14,18,40 and 43-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4-14, 18, 40 and 43-47 are pending for examination as interpreted by the examiner. The amendment and arguments filed as an RCE on 1/14/08 were considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-7, 9-14, 18, 40, and 43-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217.

Regarding claim 1, Kaku et al. teaches a high-speed optical recording apparatus in an optical storage device for generating a write signal according to an RLL modulation waveform (NRZ signal) inputted to the high-speed optical recording apparatus, so as to control a writing power of a pickup in the optical storage device (see abstract), the recording apparatus comprising: a clock generator (modulation circuit of element 7 in figure 2) for generating a first clock signal (chCLK) and a second clock signal different from the first clock signal (SCLK); an adjustment data storage unit (part of the write strategy control unit of element 104 of figure 2) for storing a plurality of sets of write strategy parameters, and selecting and outputting a corresponding set of write strategy parameters from plurality of the sets of write strategy parameters according to

the RLL modulation waveform (explained in column 5, lines 40-54). Kaku et al. also teaches in figure 2 a delay adjustment state machine (part of element 114) receiving the second clock signal (received through the output of the serial interface unit of element 100) and the selected set of write strategy parameters (done through part of write strategy of element 104), the delay adjustment state machine (element 114 of figure 2) for generating a rough delay parameter and a fine delay parameter according to the selected set of write strategy parameters, and for delaying the RLL modulation waveform according to the second clock signal and the set of write strategy parameters so as to generate a second delay signal (column 2, lines 38-40). Kaku et al. does not but Kato et al. teaches a rough delay counter or a rough delay shift register (element 322) receiving the first clock signal (through element 320), the second delay signal, and the rough delay parameter (N1), the rough delay counter or a rough delay shift register (element 322) for delaying the second delay signal according to the first clock signal and the rough delay parameter so as to generate the first delay signal. Kato et al. also teaches in figure 3 a fine delay chain (element 324) receiving (through element 322) the first delay signal and the fine delay parameter, the fine delay chain for delaying the first delay signal according to the fine delay parameter so as to generate the write signal (column 5, lines 6-19), the fine delay chain having a plurality of serially connected delay cells, each delay cell delaying an input (the first delay) signal by a predetermined period (column 5, lines 41-56). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the delay circuit of Kaku et al. of an optical recording apparatus by including the fine delay chain and specific parameters as taught

by Kato et al. for the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claims 4, Kaku et al. teaches the high-speed optical recording apparatus wherein clock generator comprises a phase locked loop for generating the first clock signal (element 115 of figure 2), and a frequency divider for dividing a frequency of the inputted first clock signal to generate the second clock signal (SCLK outputted from element 6 of figure 2). For further explanation, see column 2, lines 18-32 and column 6, lines 44-49.

Regarding claims 5, Kaku et al. teaches in figure 3 the high-speed optical recording apparatus wherein a period of the second clock signal (CLK SIGNAL) is equal to a base period of the RLL modulation waveform (NRZ SIGNAL). The equivalence is shown in figure 3 (ii) as compared to figure 3 (iv).

Regarding claims 10, Kaku et al. teaches the high-speed optical recording apparatus further comprising an EFM input interface (write strategy control unit of element 104 of figure 2) for receiving the RLL modulation waveform and generating an address signal ("timing signal" as explained in column 5, lines 40-46 serves the same purpose).

Regarding claims 12, Kaku et al. teaches the high-speed optical recording apparatus of claim 10 wherein the rough delay unit (element 114 of figure 2) is electrically connected to the EFM input interface to receive the RLL modulation waveform (shown in figure 2).

Regarding claims 13, Kaku et al. teaches in column 5, lines 36-46, the high-speed optical recording apparatus of claim 10 wherein the adjustment data storage unit (consists of the Pa-Pd registers) is electrically connected to the EFM input interface (write strategy control unit) to receive the address signal (timing signal) for selecting the corresponding write strategy parameter according to the address signal.

Regarding claims 14, Kaku et al. teaches in figure 2 the high-speed optical recording apparatus of claim 2 further comprising a data storage setting interface (duties performed by the "write strategy control unit" of element 104) electrically connected to the adjustment data storage unit (registers Pa-Pd, elements 106-109), and further electrically connected to a microprocessor of the optical storage device (through the "modulation ckt" of element 7, which is connected to the host computer of the optical storage device as shown in figure 1) to receive the sets of write strategy parameters (various recording powers) and storing the sets of write strategy parameters into the adjustment data storage unit.

Regarding claims 18, Kaku et al. teaches the high-speed optical recording apparatus of claim 1 wherein the RLL modulation waveform is generated by an EFM encoder of the optical storage device (column 4, lines 3-5 explain that the EFM code corresponds to the CD format, suggesting that the EFM code unique to the format is generated by the optical storage device).

Regarding claims 6, Kaku et al. in view of Kato et al. teaches the high-speed optical recording apparatus. Kato et al. further teaches wherein a period of the second clock signal is equal to a multiple of a period of the first clock signal (column 6, lines 37-

44). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the delay elements of Kato et al. into the delay circuit of Kaku et al. This serves the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claims 7, Kaku et al. in view of Kato et al. teaches in the high-speed optical recording apparatus. Kato et al. further teaches in column 2, lines 37-40 wherein a resolution of the delay adjustment state machine delaying the RLL modulation waveform (amount of delay for the EFM data pulse edges) is equal to a period of the second clock signal (code rate clock). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the delay elements of Kato et al. into the delay circuit of Kaku et al. This serves the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claims 9, Kaku et al. in view of Kato et al. teaches the high-speed optical recording apparatus. Kato et al. further teaches wherein a resolution of the rough delay counter delaying the second delay signal is equal to a period of the first clock signal (column 2, lines 49-55). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the delay elements of Kato et al. into the delay circuit of Kaku et al. This serves the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claims 11, Kaku et al. in view of Kato et al. teaches the high-speed optical recording apparatus. Kato et al. further teaches wherein the EFM input interface generates the address signal according to a previous land section, a current pit section,

and a next land section in the RLL modulation waveform (column 4, lines 9-18 and column 5, lines17-19). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the clock signal dependencies and generation of the address signal of Kato et al. into the invention of Kaku et al. The given structure of delays provides robust and stable delays that are independent of temperature, voltage, and process variations (column 2, lines 41-43 of Kato et al.). The given structure of generating the address signal allows for programmability of values that are dependent on the CD-RW manufacturer (column 5, lines 20-28 of Kato et al.). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the delay elements of Kato et al. into the delay circuit of Kaku et al. This serves the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claim 40, Kaku et al. teaches a high-speed optical recording apparatus in an optical storage device for generating a write signal according to an RLL modulation waveform (NRZ signal) inputted to the high-speed optical recording apparatus, so as to control a writing power of a pickup in the optical storage device (see abstract), the recording apparatus comprising: a clock generator (modulation circuit of element 7 in figure 2) for generating a first clock signal (chCLK); an adjustment data storage unit (part of the write strategy control unit of element 104 of figure 2) for storing a plurality of sets of write strategy parameters, and selecting and outputting a corresponding set of write strategy parameters from plurality of the sets of write strategy parameters according to the RLL modulation waveform (explained in column 5, lines 40-

54); a rough delay unit (delay circuit of element 114 of figure 2) electrically connected to the clock generator to receive the first clock signal, and further electrically connected to the adjustment data storage unit to receive the selected set of write strategy parameters, the rough delay unit (element 114 of figure 2) for generating a fine delay parameter according to the selected set of write strategy parameters, and for delaying the RLL modulation waveform according to the first clock signal and the selected set of write strategy parameters to generate a first delay signal (column 2, lines 38-40). Kaku et al. does not but Kato et al. teaches in figure 3 a fine delay chain (element 324) electrically connected to the rough delay unit (element 322) to receive the first delay signal and the fine delay parameter, the fine delay chain for delaying the first delay signal according to the fine delay parameter so as to generate the write signal (column 5, lines 6-19), the fine delay chain comprising a plurality of serially connected delay cells, each delay cell delaying an input (the first delay) signal by a predetermined period (column 5, lines 41-56). Kato et al. teaches that the fine delay chain is not connected to and does not utitlize a clock signal for delaying the first delay signal to generate the write signal. Column 5, lines 29-40 explain how delay parameters can be generated without the use of a clock signal. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the delay circuit of Kaku et al. of an optical recording apparatus by including the fine delay chain and specific parameters as taught by Kato et al. for the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claim 43, Kaku et al. in view of Kato et al. teaches the high-speed optical recording apparatus. Kato et al. further teaches in figure 5 wherein the delay cells within the fine delay chain are inverters. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the delay elements of Kato et al. into the delay circuit of Kaku et al. This serves the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claim 44, Kaku et al. in view of Kato et al. teaches the high-speed optical recording apparatus. Kato et al. further teaches in figure 5 wherein the delay cells within the fine delay chain are buffers (the ability of each amplifier to provide electrical impedance transformation from one circuit to another allows them to act as buffers). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the delay elements of Kato et al. into the delay circuit of Kaku et al. This serves the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claim 45, Kato et al. teaches the high-speed recording apparatus, wherein the fine delay chain is not connected to and does not utilize a clock signal for delaying the first delay signal to generate the write signal. Column 5, lines 29-40 explain how delay parameters can be generated without the use of a clock signal. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the delay elements of Kato et al. into the delay circuit of Kaku et al. This serves the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

Regarding claim 46, Kaku et al. in view of Kato et al. teaches the high-speed recording apparatus. Kato et al. further teaches wherein the fine delay chain (shown in figure 5) is for delaying the first delay signal only according to the fine delay parameter so as to generate the write signal (column 5). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the delay elements of Kato et al. into the delay circuit of Kaku et al. This serves the purpose of helping to accurately generate delays in write pulses at high speeds (column 2, lines 24-31 of Kato et al.).

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaku et al. in view of Kato et al., as applied to claim 1 above, and further in view of Chung et al., US Patent 4,873,680.

Kaku et al. in view of Kato et al. teaches the high-speed optical recording apparatus of claim 1. In addition, Kato et al. teaches the high-speed optical recording apparatus wherein the rough delay counter comprises a counter. In column 2, lines 49-51, the EFM data is said to pass through a four stage shift register for a course delay. This is equivalent to passing the data through a four-bit counter for a rough delay. Although there is no comparator in the system, the rough delay element of 322 in figure 3 takes in the same parameters as the comparator to output the same type of delay signal.

Kaku et al. as modified by Kato et al. does not specifically teach a comparator to compare the value of the rough delay signal and the output signal of the counter.

Chung et al. teaches in figure 15, a comparison circuit (element 240) connected to a shift register (element 242) for the same general purpose.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the concept of the given shift register as taught by Chung et al. into the system of Kaku et al. in view of Kato et al. This would serve the purpose of increasing accuracy and reliability of data storage and retrieval (column 2, lines 36-40 of Chung et al.).

4. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217 in view of Han, US Patent 7,102,976.

Regarding claim 47, Kaku et al. in view of Kato et al. teaches the high-speed optical recording apparatus. Kato et al. further teaches wherein the fine delay chain further comprising a multiplexer having inputs coupled to the outputs of the delay cells, a selecting end coupled to the fine delay parameter, and an output end being coupled to the write signal, the multiplexer for generating the write signal being one of the outputs of the delay cells as selected according to the fine delay parameter (the selection method given in column 5 serves the same purpose of selecting the delay parameter based on the output of the delay cells to generate the write signal). Kaku et al. in view of Kato et al. does not give the specifics of the multiplexer. Kaku et al. in view of Kato et al. does not but Han teaches in figure 3 (which is explained in column 5) the fine delay chain ("ring oscillator") further comprising a multiplexer (320) for selecting the write signal from a plurality of outputs of the inverters or buffers (300). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the concept of using a multiplexer to select signals as taught by Han into the system of

Kaku et al. in view of Kato et al. The motivation would be to generate a write pulse using an apparatus that requires less time and effort to develop (column 1, lines 63-67 of Han).

Response to Arguments

5. Applicant's arguments filed 1/14/08 have been fully considered but they are not persuasive.

Applicant argues that Kaku et al. does not teach a delay adjustment state machine. However, element 114 of figure 2 performs the same function.

Applicant argues that Kaku et al. does not teach that the internal data bus transfers the clock signal to the write strategy control unit. However, as the data utilizes this clock (it is the only one feeding into element 100) the internal data bus also carries the same clock signal.

Applicant argues that Kaku et al. fails to disclose that the delay adjustment state machine delays the RLL modulation waveform according to the second clock and the set of write strategy parameters. However, figure 2 shows how the second clock is used in the internal data bus feeding into element 104, which has the write parameters. These are utilized in the delay of element 114.

Applicant argues that Kato et al. teaches not utilizing a clock signal for generating delay parameters, but does not teach not utilizing a clock signal for delaying the first delay, clarifying the difference between generation and utilization. However, by not utilizing a clock signal in the generation of the delay parameters, Kato et al. does not

utilize a clock signal in delaying the first delay. If no clock signal was utilized in generating a delay parameter, no clock signal can be utilized while the parameter is implemented. Although one delay is used for the other delay in the present application, both are dependent upon the first clock. The present claim language does not recite that the delay signal is delayed solely through the use of another delay signal. By using the first delay signal utilizing a clock to delay the second delay signal, the second delay signal is indirectly utilizing the same clock.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Parul Gupta whose telephone number is 571-272-5260. The examiner can normally be reached on Monday through Thursday, from 9:30 AM to 7 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch can be reached on 571-272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/PHG/
2/20/08

/William Korzuch/
SPE, Art Unit 2627